CALCULATOR-BASED SYNTHESIS ROUTINE SPEEDS MICROWAVE AMPLIFIER DESIGN

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Abstract

A calculator-based synthesis routine provides rapid and accurate design of interstage networks of prescribed gain, bandwidth, ripple and slope for use in microwave amplifiers. The complete design and measurement of a prototype 6—12 GHz amplifier illustrates the computer-aided synthesis approach to microwave amplifier design.

I. Introduction

Traditionally microwave amplifiers have been designed using Smith Chart or other graphical cut-and-try approaches. These methods are extremely time consuming and provide no guarantee of an optimum solution. Recently techniques have been developed for the direct synthesis of interstage networks[1-2] which allow rapid and accurate design of interstage networks. The computer aids for the direct synthesis of interstage networks has, however, not found widespread distribution. This paper describes the features and illustrates the use of an available calculator-based synthesis routine capable of synthesizing interstage networks of prescribed gain, bandwidth, ripple, slope, impedance transformation, and parasitic element inclusion. The calculation procedures of the synthesis routine are described and illustrated and the use of the routine in a complete microwave amplifier design is illustrated. Finally, the measured performance of the synthesis-designed microwave amplifier is compared to theoretical predictions.

II. Calculation Procedure for Synthesis of Interstage Networks

A brief outline of the synthesis calculation process is here presented to provide insight into the straightforward computational process whereby passive interstage networks of prescribed frequency response are obtained. Figure 1 defines the insertion loss function (IL) to which a network is to be synthesized. For a network to be synthesized from a given insertion loss function it is only necessary that:

a) The IL be bounded for all ω:

$$1 \leq IL \leq \infty \quad \text{for } 0 \leq \omega \leq \infty$$

and b) The chosen topology be consistent with the given IL form.

When the above conditions hold, the following procedure produces a network having the frequency response of the Insertion Loss function (IL):

1. Form an insertion loss function that exhibits the desired frequency response. This is the APPROXIMATION PROBLEM and techniques have been developed for obtaining an insertion loss function of specified gain, gain slope, bandwidth and ripple[2]. For networks without antiresonant circuits (trapless filters) the insertion loss function takes the form:

$$IL = \frac{a_0 + \ldots a_{2N}\omega^{2N}}{\omega^{2J}}$$

N = Network Order
J = Number of high pass elements

2. From $IL(\omega) = \frac{a_0 + \ldots a_{2N}\omega^{2N}}{\omega^{2J}}$

compute $|\rho_1(\omega)|^2 = 1 - 1/IL(\omega)$

3. Substitute

$$\omega = s/j \text{ to obtain } |\rho_1(s)|^2 = \rho_1(s)\rho_1(-s)$$

4. Obtain the zeros and poles of $|\rho_1(s)|^2$

5. Form

$$\rho_1(s) = \frac{\pm 1 \prod_{i=1}^{N} (s-z_i)}{\prod_{i=1}^{N} (s-p_i)}$$

Where the poles of $\rho_1(s)$ are the poles of $|\rho_1(s)|^2$ that are in the left half plane (LHP) and the zeros of $\rho_1(s)$ are chosen from the zeros of $|\rho_1(s)|^2$ in complex pair fashion but otherwise can be LHP or RHP.

6. Form $z_1(s) = R_1 \frac{1 + \rho_1(s)}{1 - \rho_1(s)}$

7. Determine the network element values by forming the appropriate expansion of $z_1(s)$ about zero and infinity.

8. Scale the synthesized network to the actual source impedance and operating frequency.

9. Perform internal impedance transformations within the synthesized network to obtain the desired termination.

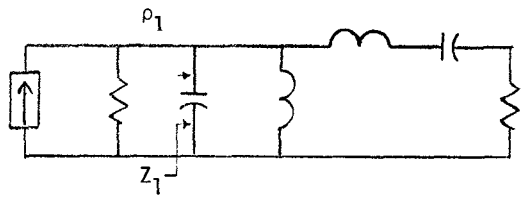
III. Example of Synthesis Computations

The synthesis computations are here illustrated by a simple example. The numbered steps of this example correspond to the outlined steps of the previous section.

1. An interstage is to be designed to operate between a 124Ω source and 11.4Ω load with 6 dB/octave gain slope and .4 dB ripple over 6 to 12 GHz. The following insertion loss function (normalized to upper cut-off of 1 radian/sec) is obtained via the methods of [2]:

$$IL = \frac{.80 - 5.8\omega^2 + 19.9\omega^4 - 23.9\omega^6 + 10.1\omega^8}{\omega^4} \; **$$

and the chosen topology is



2. $|\rho_1(\omega)|^2 = \frac{.8 - 5.8\omega^2 + 18.9\omega^4 - 23.9\omega^6 + 10.1\omega^8}{.8 - 5.8\omega^2 + 19.9\omega^4 - 23.9\omega^6 + 10.1\omega^8}$

3. $|\rho_1(S)|^2 = \frac{.8 + 5.8S^2 + 18.9S^4 + 23.9\omega^6 + 10.1\omega^8}{.8 + 5.8S^2 + 19.9S^4 + 23.9\omega^6 + 10.1\omega^8}$

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**In actual practice, computations should be carried out to more significant figures than is shown here.

4. poles of $|\rho_1(S)|^2$: $S = \pm.19 \quad \pm j.48$

$S = \pm.19 \quad \pm j\ 1.01$

zeros of $|\rho_1(S)|^2$: $S = \pm.18 \quad \pm j.51$

$S = \pm\ 0 \quad \pm j.98$

5. The multiplier for ρ_1 is taken as negative to assure consistency with the topology and the zeros of ρ_1 are chosen to be RHP:

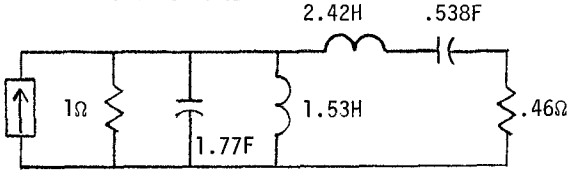
$$\rho_1 = \frac{(-1)(S + j.98)(S - j.98)(S - .18 + j.51)(S - .18 - j.51)}{(S + .19 + j.48)(S + .19 - j.48)(S + .19 + j1.01)(S + .19 - j1.01)}$$

$$\rho_1 = \frac{-S^4 + .36S^3 - 1.2S^2 + .36S - .28}{S^4 + .74S^3 + 1.4S^2 + .50S + .28}$$

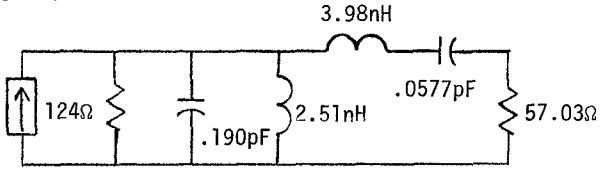
$$Y_1 = 1/Z_1 = \frac{2S^4 + .38S^3 + 2.7S^2 + .14S + .56}{1.1S^3 + .21S^2 + .86S}$$

$$Y_1 = 1.77S + \frac{1}{1.53S} + \frac{1}{2.42S + \dfrac{1}{.538S} + .46}$$

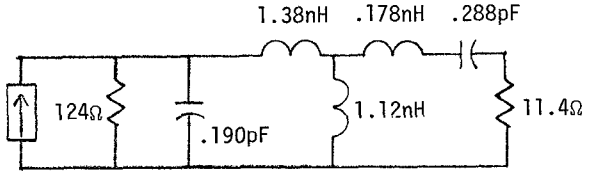
The synthesized network is then:



8. The network is scaled to 124 ohm source and 12 GHz upper cut-off frequency:



9. The shunt-series connection of inductors is used to affect the desired impedance transformation. The result is a TEE of inductors[3] and impedance level shifting to the right of the inductor TEE:



Note that this interstage is used in the complete amplifier design of section V.

IV. NETSYN: Complete Interstage Synthesis in a Calculator Based Routine

The computations described and illustrated for the synthesis of passive networks of prescribed frequency response are readily amenable to CAD programming ahd have been implemented in a CAD routine called NETSYN. This HP 9830 calculator-based synthesis routine performs all of the calculations in the synthesis process and provides interstage networks to user specifications. The program features:

1. Synthesis of lossless coupling networks of prescribed ripple, bandwidth and gain versus frequency slope.

2. Accurate synthesis of networks containing up to 10 reactive elements.

3. Automatic checking of user-specified network topologies to assure consistency with frequency response specifications.

4. Adjustment of the frequency response to assure inclusion of prescribed parasitic elements.

5. Automated implementation of internal impedance transformations to obtain a desired load impedance.

The NETSYN Program thus provides the necessary tools for rapid and accurate design of interstage networks for microwave amplifiers.

V. Complete Amplifier Design Example Using Synthesized Matching Networks

A complete amplifier design is here undertaken to illustrate how a complete microwave amplifier can be designed from transistor S-parameters and amplifier specifications using the NETSYN program to synthesize interstages of desired frequency response. The synthesized networks are transformed to transmission line equivalents suitable for realization in microstrip form, and the measured performance of the amplifier is compared to design predictions.

The interstage design steps of Figure 2 are followed in the design of a two stage GaAs FET power amplifier covering 6 to 12 GHz. The representative S-parameters of Figure 3 are used for the amplifier design calculations.

Figure 4 shows the unilateral, lumped model of the GaAs FET characteristics used in design process. This model was chosen to provide most exact agreement with measured parameters at 12 GHz but the model agrees very closely with measured parameters both in impedance and gain characteristics over the entire 6—12 GHz band. The next step is to synthesize interstage networks which provide the desired gain characteristics and can incorporate input and/or output impedance of the GaAs FET. The NETSYN program was used to obtain the synthesized interstage networks of Figure 4 to the following specifications:

Input Matching Network

Gain slope	6 dB/octave
Ripple	.4 dB
Minimum Insertion Loss	0 dB

Interstage Matching Network

Gain slope	6 dB/octave
Ripple	.4 dB
Minimum Insertion Loss	0 dB

Output Matching Network

Gain slope	0 dB/octave
Ripple	.04 dB
Minimum Insertion Loss	.025 dB

The circuit of Figure 4 is called the ideal amplifier because it is based on a lumped, unilateral model of the transistor and lumped elements for the interstage networks. For realization the lumped elements of the interstage networks are approximated by transmission line equivalents. Series and shunt inductors can be approximated by transmission lines of highest realizable characteristic impedance (Z_{OH}) and lengths given by

$$\ell = (V/\omega_U)\tan^{-1}(\omega_U L/Z_{OH}) \qquad (1)$$

where ℓ is the length of line, ω_U is the upper passband frequency, L is the inductance to be approximated, and V is the speed of light in the

transmission medium.

A similar technique approximates shunt capacitors with open shunt stubs of lowest feasible characteristic impedance (Z_{0L}) and length:

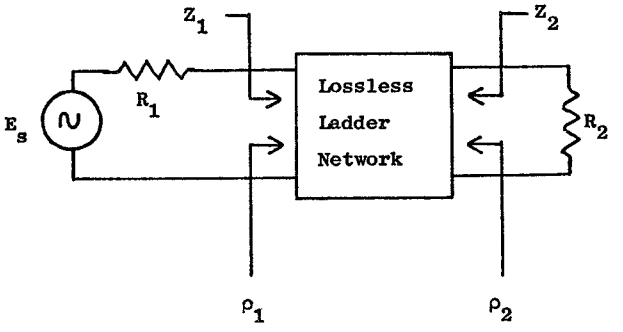
$$\ell = (V/\omega_U)\tan^{-1}(\omega_U C Z_{0L}) \qquad (2)$$

Using $Z_{0H} = 110\Omega$, $Z_{0L} = 25\Omega$ and $V = 1.2 \times 10^{10}$cm/sec, the circuit of Figure 5 was obtained. This circuit is termed the [S]-distributed realization of the amplifier because actual S parameters and distributed matching networks are used in this circuit.

A microstrip construction of the GaAs FET amplifier is shown in Figure 6. The gain response of the amplifiers of Figures 4, 5 and 6 are compared in Figure 7. Circuit losses, wafer to wafer transistor gain variations and common lead inductance are not accounted for in the [S]-distributed amplifier and are responsible for the reduced gain in the actual amplifier.

VI. Conclusions

Computer Aided insertion loss synthesis provides a rapid and accurate method for interstage design in wideband microwave amplifiers. From a user-specified gain, bandwidth and ripple, lumped-element interstage networks can be obtained and transformed to transmission line realizations suitable for microstrip construction. Synthesis-designed microwave amplifiers exhibit performance in excellent agreement with design predictions.



$$\rho_1 = \frac{Z_1 - R_1}{Z_1 + R_1} \qquad IL = \frac{P_{AV} \text{ from } E_s, R_1}{P_{del} \text{ to } R_2}$$

Figure 1. Schematic and Definitions for Insertion Loss Synthesis

VII. Acknowledgement

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VIII. References

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2. D. J. Mellor and J. G. Linvill, "Synthesis of Interstage Networks of Prescribed Gain Versus Frequency Slopes," IEEE Trans. Microwave Theory Tech., vol. MTT-23, pp. 1013-1020, Dec. 1975.

3. G. A. Vincent, "Impedance Transformation Without A Transformer", Frequency Technol., vol. 7, pp. 15-21, Sept. 1969.

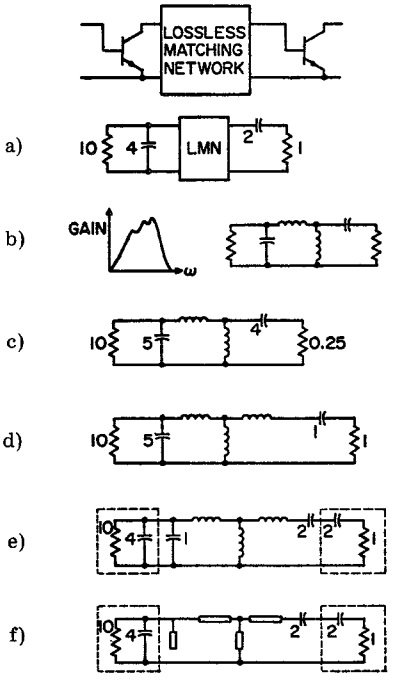

Figure 2. Outline of matching synthesis procedure. (a) Model device impedances (b) Constrain frequency response and select topology consistent with parasitic elements. (c) Synthesize network. (d) Transform impedance (e) Separate out device impedances. (f) Transform design to transmission-line equivalent.

[S] =

FREQ.	S_{11} MAG	S_{11} ANG	S_{12} MAG	S_{12} ANG	S_{21} MAG	S_{21} ANG	S_{22} MAG	S_{22} ANG
6.000	0.769	-97.0	0.069	39.0	2.771	104.0	0.486	-48.0
9.000	0.705	-122.5	0.070	31.0	1.955	82.7	0.496	-65.7
12.00	0.678	-132.0	0.066	33.0	1.427	69.0	0.564	-71.0

FREQ.	K	GA MAX	GU MAX	GAMMA MS		GAMMA ML	
6.000	0.796	INF	13.910				
9.000	1.268	11.350	10.039	0.830	128.3	0.714	80.9
12.00	1.784	8.215	7.425	0.758	137.0	0.675	79.7

PLOT:

Figure 3. S parameters of GaAs FET.

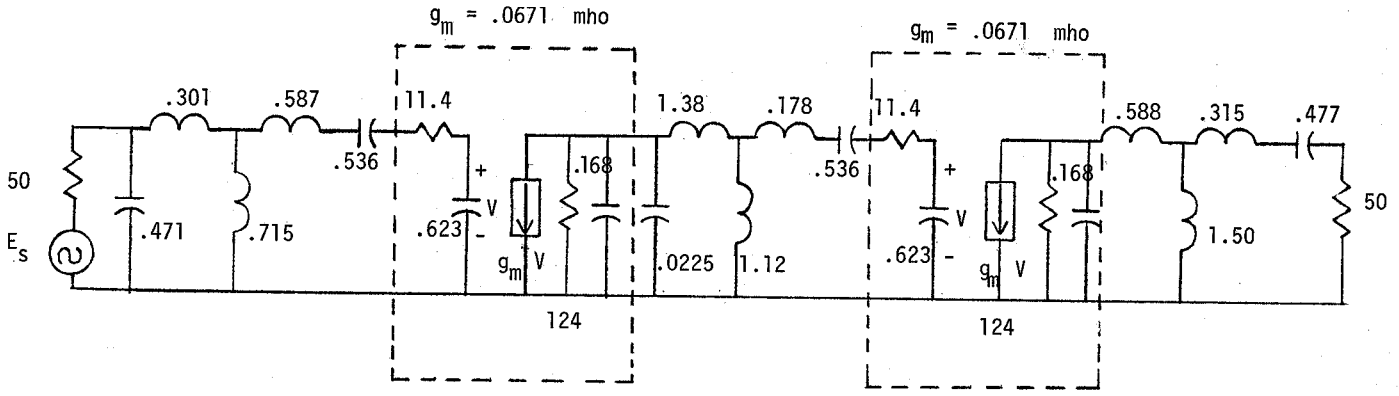

Figure 4. Schematic of Ideal Amplifier using a unilateral lumped model for the GaAs FET and lumped interstage network. Units are ohms, pF, nH.

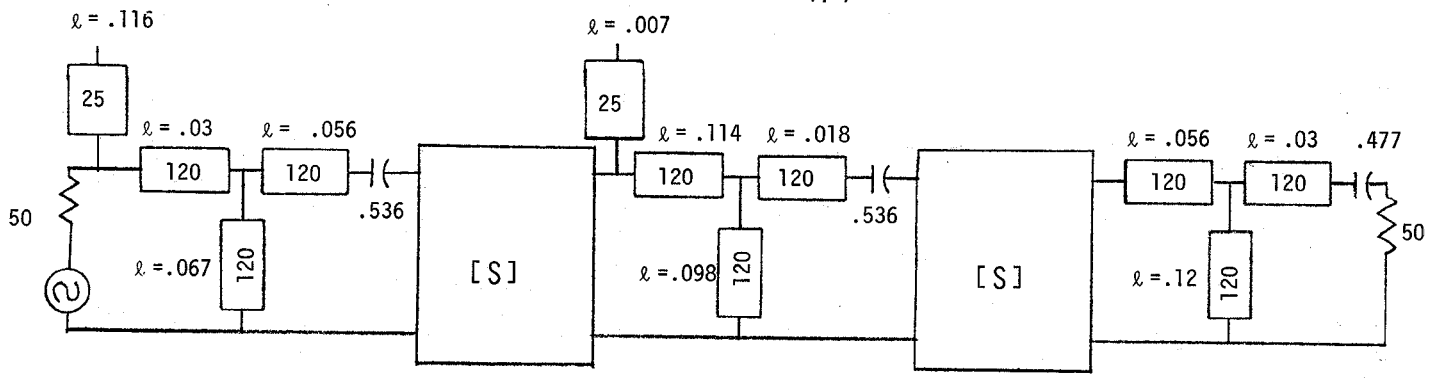

Figure 5. Schematic of [S] - distributed amplifier using actual S parameters and distributed realizations of interstage networks. Units are ohms, pF, cm.

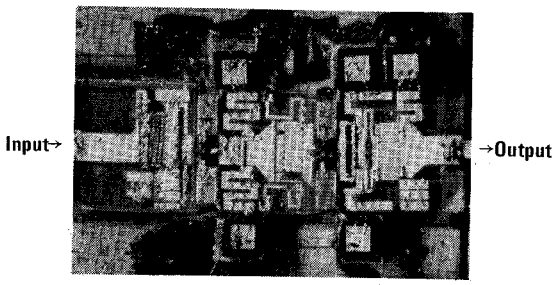

Figure 6. Photograph of 6 - 12 GHz Prototype Amplifier.

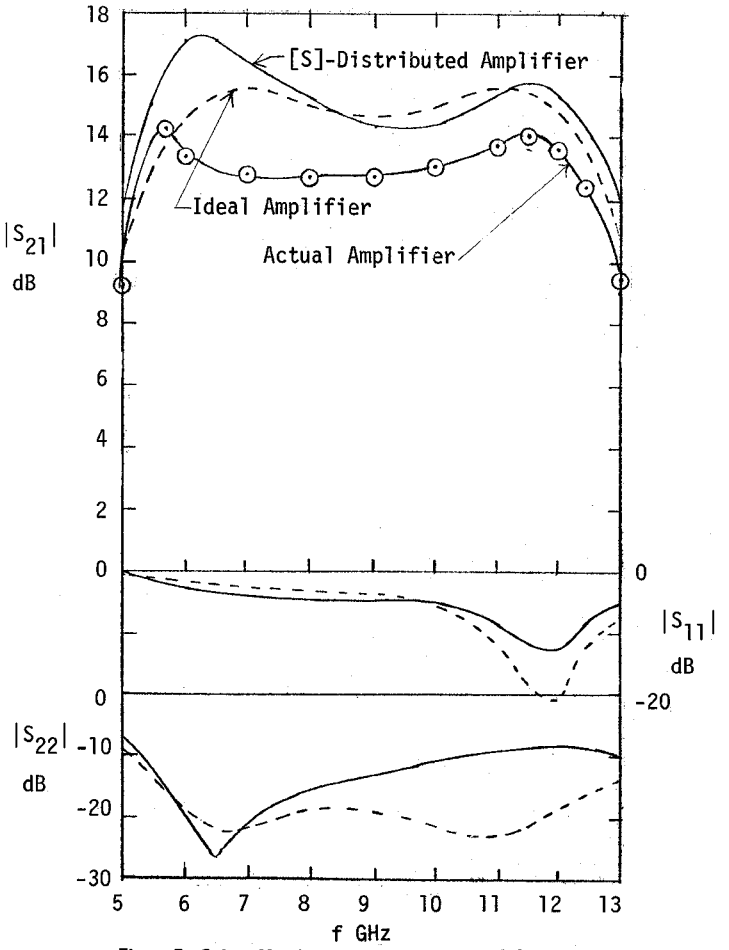

Figure 7. Gain + Match Comparisons of Ideal. [S] - Distributed Amplifiers, and Actual Amplifiers